



UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

STEPHEN FULD

Serial No.: 09/479,146

Filed: January 7, 2000

For: METHOD AND SYSTEM FOR RECONSTRUCTING
DATA SERIALY ARRANGED ON A MAGNETIC TAPE TRACK (As Amended)

Attorney Docket No.: 99-051-TAP (STK 99051 PUS)

Group Art Unit: 2184

Examiner: Michael Maskulinski

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REPLY BRIEF UNDER 37 C.F.R. § 1.193 RECEIVED

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Sir:

This Reply Brief is in reply to the Examiner's Answer mailed on September 11, 2003. The Examiner's Answer is in response to the Appeal Brief mailed by the Applicant on August 1, 2003.

Applicant's Reply to (11) Examiner's Response to Argument

As noted by the Examiner in the (11) Response to Argument of the Examiner's Answer, the Applicant has argued that White does not teach or suggest data blocks and a parity block serially arranged on a magnetic tape track with the parity block following the data

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blocks in the manner of the RAID-4 standard as claimed; and the Applicant has further argued that White teaches blocks serially arranged on a magnetic tape track with some of the blocks being data blocks and some of the blocks being data and ECC blocks.

The Examiner disagreed with the Applicant's arguments and posited that the illustration on the bottom of page 176 of White teaches that "the EC blocks are grouped together and that they are not both data and EC blocks" and that point 5 on page 176 of White teaches that of the blocks in a segment of 32 blocks, eight of these blocks contain error-correction codes (ECC). The illustration on page 176 of White shows a tape track having a segment of blocks. The relevant portion of point 5 on page 176 of White is as follows:

Of the [32] blocks in a segment, eight contain error-correction codes. In addition, at the end of each block, the drive computes a *cyclic redundancy check* (CRC) for further error correction and appends it to the block.

As such, the illustration and point 5 on page 176 of White teaches that certain blocks contain ECC. The Applicant has argued that such blocks are "data and ECC blocks." Further, appended to each block is a CRC. Accordingly, there are two types of blocks in a segment: 1) "data and ECC blocks"; and 2) "data, ECC, and CRC blocks." Notably, there is no block in the segment containing only data, i.e., there is no "data block"; and there is no block in the segment containing only error correction information, i.e., there is no "parity block". In contrast to White, the claimed invention is directed to data blocks and a parity block being "serially arranged on a track of the magnetic tape with the parity block following the data blocks and the parity block being based on the data blocks."

The Examiner posited that the illustration at the top of page 177 of White teaches "DATA bits followed by EC bits." The Examiner posited that point 2 on page 177 of White teaches "a [RAM] buffer used to prepare data that is written onto the tape" and teaches that the RAM buffer is dumped to the controller's buffer which appends error correction (EC) codes if the controller has chips that handle error correction; and further

teaches that “if the controller doesn’t have built-in error correction, the software computes the EC codes based on the pattern of 0 and 1 bits in the files, *and appends them to the end of the data* (emphasis by the Examiner) in the RAM buffer” with the contents of the RAM buffer being copied to the controller buffer.

The Applicant agrees that the illustration at the top of page 177 of White teaches data bits followed by EC bits. The Applicant further agrees that the EC codes (i.e., ECC) are appended to the end of the data bits. However, the Applicant posits that the EC codes appended to the end of the data bits form one block containing both data and EC codes, i.e., a “data and ECC block.” Support for the Applicant’s position is found in point 2 on page 177 of White:

Once the data is transferred to the controller, the RAM buffer is free to receive the next block of data from the disk.

As described in point 2 on page 177 of White, the data transferred to the controller from the RAM buffer may be a data block in which the controller appends the ECC. The result is a “data and ECC block.” As described in point 2 on page 177 of White, if the controller does not have ECC capability, then software computes the ECC and appends them to the data block in the RAM buffer in which the contents of the RAM buffer are copied to the controller. The copied contents is a “data and ECC block.”

Further support for the Applicant’s position is found in the “Restoring Files” section at the bottom of page 177 of White which describes that “the EC codes appended to each data block” may be used to fix the data in case of error. As such, “the EC codes appended to each data block” form “data and ECC blocks” as opposed to “data blocks” and “a parity block” as claimed.

Accordingly, White does not teach or suggest data blocks and a parity block serially arranged on a track of the magnetic tape with the parity block following the data blocks in the manner of the RAID-4 standard as claimed. Therefore, modifying Stolowitz with White would not result in the claimed invention.

For these and other reasons contained in the Appeal Brief, the Applicant respectfully submits that claims 12-14 and 16-18 are patentable under 35 U.S.C. § 103(a) over Stolowitz and White.

Respectfully submitted,

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